Abstract

This study focuses on designing a low-noise, high-speed integrator charge pump for Phase-Locked Loop (PLL) for 7G WiFi. To provide a steady and noiseless frequency as a reference clock for other units, PLLs require a ripple-free control voltage for their internal oscillator. The conventional charge pump circuit, which relies on cascoded CMOS switches for generating the control voltage, introduces numerous non-ideal characteristics that result in undesired fluctuations in the voltage. Common issues with this topology, including current mismatch, RC filter noise, and charge sharing, are addressed and resolved by completely eliminating the conventional switch-mode charge pump and replacing it with an active non-inverting differential integrator for the equivalent integration operation. Designed and simulated with TSMC 65nm technology, the integrator charge pump circuit successfully operates in the 7G WiFi frequency band, and even at higher frequencies with a power consumption of 1.6mW. Although the power consumption may increase due to the inclusion of active components, the proposed design substantiates its ability to remove undesired voltage variation, operate at high frequencies, and reduce the complexity of the design by eliminating the inversion delay previously needed for driving the CMOS switches.