Abstract

At the heart of any RF communication system is a carrier frequency synthesizer, usually an analog PLL. This PLL acts as a a phase/frequency amplifier, amplifying an input f_{ref} signal depending on some feedback divider ratio. The PLL is composed of a PFD, Charge Pump, Loop Filter, VCO, and feedback divider. All these components must be optimized to minimize phase noise within some power and settling time constraints. In the following work a Quadrature VCO was designed with minimal phase noise and power consumption. A novel current-steering charge pump was introduced and simulated to have lower transient spiking and settling time than alternative topologies common in literature. All these blocks were modeled together to achieve a phase noise and power consumption in line with state-of-the-art performance.